Microwave Inductors and Capacitors in Standard Multilevel Interconnect Silicon Technology

Joachim N. Burghartz, *Senior Member, IEEE*, Mehmet Soyuer, *Member, IEEE*, and Keith A. Jenkins

Abstract—**Spiral inductors and metal-to-metal capacitors for microwave applications, which are integrated on a silicon substrate by using standard 0.8 μm BiCMOS technology, are described. Optimization of the inductors has been achieved by tailoring the vertical and lateral dimensions and by shunting several interconnect metal layers together. Lumped element models of inductors and capacitors provide detailed understanding of the important geometry and technological parameters on the device characteristics. The high quality factors of nearly 10 for the inductors are among the best results in silicon, particularly when using standard silicon technology.**

I. Introduction

MONOLITHIC MICROWAVE integrated circuits (MMIC's) are rapidly outpacing discretes in mobile wireless communication products [1]. The maturity, high integration level, and low-cost aspects of silicon technology make particularly Si-BiCMOS a serious contender for this high-volume market. Besides its superiority at intermediate frequencies (IF), the advent of SiGe-HBT's in submicrometer, self-aligned structures allows silicon technology to cope well with GaAs at microwave and millimeterwave frequencies [2], [3]. The major concern about the use of silicon are the high substrate losses due to the much lower substrate resistivity compared to GaAs. Also, aluminum-copper (AlCu) interconnects are typically used, which have a higher resistivity than the gold (Au) metalization used in GaAs technology, and the metal thickness is also smaller than in GaAs. Transmission line fabrication and the design of high-Q inductors and capacitors are therefore difficult tasks in standard silicon technology. Although substrate losses can be considerably reduced by using high-resistivity (HRS) or silicon-on-insulator (SOI) substrates [4], the results and discussions in this paper will show that high-Q inductor and capacitor designs are possible even in standard silicon technology.

In Section II, the fabrication process of the experimental inductors and capacitors is described, and in Section III the measurement results are summarized, models for inductors and capacitors are presented, and the parameter impacts are discussed. Section IV gives conclusions and provides an outlook on possible future developments and trends.

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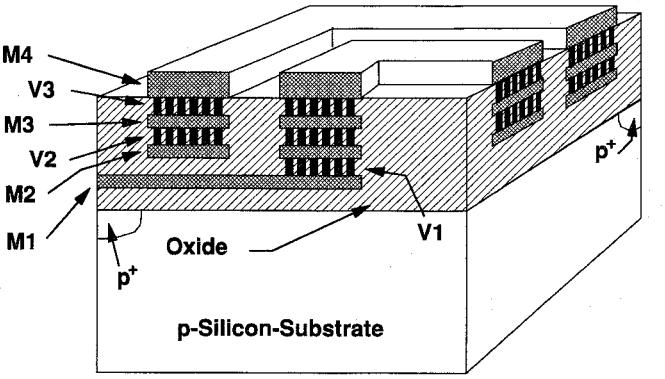

Fig. 1. Cross-sectional view of the four level interconnect scheme provided with the 0.8 μm BiCMOS technology which was used. The center section of a spiral inductor structure is shown. (Note that the silicon region under the inductor was protected from any additional implant.)

II. Inductor and Capacitor Fabrication Process

A 0.8 μm BiCMOS technology with four levels of AlCu interconnects was used to fabricate various inductor and capacitor structures [5]. A cross section of the center part of a spiral inductor structure, involving all metal levels, is shown in Fig. 1. The thickness of the first (M1), second (M2), and third (M3) metal layer was about 1.0 μm, while the fourth (M4) metal layer was about 2.0 μm thick. The isolating oxide between metal layers was 1.5 μm thick, and the oxide thickness between M2 and the silicon substrate was about 4.5 μm. M2 was the lowest metal level used in the inductor and capacitor structures, except for the inductor's underpass which was at M1. The substrate resistivity under the inductors was 10 ohm-cm in most cases, but one inductor structure was also fabricated over a p-well region with a resistivity of $\sim$0.1 Ω-cm at $\sim$1.1 μm well depth. The p-well was also present under the metal-insulator-metal (MIM) capacitors.

In GaAs MMIC technology, interdigital capacitors are most commonly used because they require only one metal level and provide the small capacitance values required for microwave/millimeter wave applications [6]. Much larger capacitance values are needed in silicon VLSI technology because circuits operate at MHz frequencies. The preferred structure here is the MOS-capacitor which has a high capacitance/area ratio. The MOS-cap, however, has one silicon contact electrode, and therefore the achievable Q is relatively small. Both device structure concepts are not very well suited for L-band and S-band applications, due to a large area consumption as far as the interdigital capacitor goes, and poor parameter control

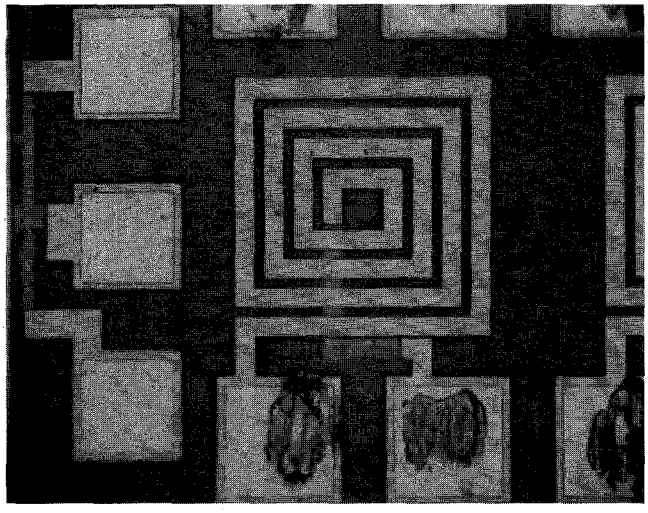

Fig. 2. Plan view photograph of the inductor M2/M3/M4 on the chip.

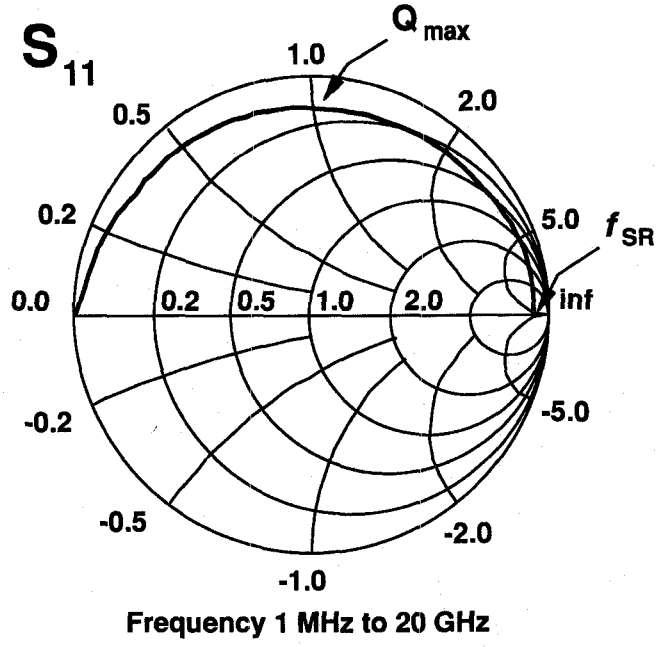

Fig. 3. Smith chart measurement results of inductor M2/M3/M4. The markers indicate the frequency of Q_{max} and the self-resonance frequency.

at small geometries and low Q's for the MOS-cap. A better solution at these frequencies is the MIM capacitor which has advantages due to the moderate capacitance/area values and high Q-factors with the two metal contacts. For this work we fabricated dual MIM-capacitors with use of the M1, M2, and M3 metal levels. For the S-parameter measurements, M2 and M3 were contacted and M1 was left floating. But it is also possible to connect M1 and M3 to form one contact and use M2 as the second contact of the dual capacitor in order to double the capacitance per area.

Inductor fabrication on a chip is typically achieved by the formation of a spiral with a square, beveled, or round footprint and with a metal underpass [7]. Thus an interconnect technology with at least two metal levels is required. Multilevel interconnects are a common feature of todays silicon VLSI technologies, but the processes developed to achieve a metal pitch of the order of a few micrometers leads to a limitation in metal thickness. This limitation results from the fact that the metal lines are dry-etched to generate micrometer-size pattern, and not structured by lift-off or similar techniques used to fabricate coarser geometries [8]. Effectively thicker metal wires can be realized in standard silicon technology by connecting multiple metal layers with dense via arrays. In this work, inductors with one (M3), two (M2/M3 or M3/M4), and three (M2/M3/M4) metal levels were built to explore this design option and to achieve high Q-factors (Table I). In all cases the underpass was at M1 to ensure that the spacing between inductor and the substate was maximum and thus substrate losses were minimum. The importance of this design aspect will be explained in Section III. The lateral dimensions of the inductors were the same, with four turns, an inductor area (footprint) of 226 × 226 μm^2, and 16 μm metal width and 10 μm metal-metal space (i.e., 26 μm metal pitch). A plan view photograph of the M2/M3/M4-inductor is shown in Fig. 2.

Inductor and capacitor structures were connected to high-frequency test pads for S-parameter analysis. The metal pads had the full pad size at the M4 level, but the via arrays and lower metal layers were limited in size to minimize the metal to substrate capacitance. Open-contact, short, and 50 Ω calibration structures were placed in close proximity to the individual sites for proper elimination of parasitics prior to the S-parameter analyses.

III. Results and Discussion

The experimental devices were characterized by using a 20 GHz HP8720B network analyzer and on-wafer measurements with microwave probes. The parasitic capacitances and the contact resistance were accurately subtracted from the measurement data with calibrations on the open, short, and 50 Ω resistor sites. The S_{11} parameter was extracted from a one-port measurement of the reflection coefficient. A smith chart of the M2/M3/M4 inductor measurement is shown in Fig. 3. The markers in this figure indicate the frequencies of maximum Q and the self-resonance frequency. The impedances Z_{in} were then derived from S_{11} versus frequency data for all inductors and the MIM capacitor. The inductor data were compared with the model in Fig. 4(a), which is similar to the one published in [9]. The capacitances C_P and C_{OX} were calculated by using an electromagnetic simulation (EMS) tool [10]. The values for the inductance L_S were also derived from EMS, and had only little frequency dependence until frequencies approached self-resonance. The series resistance of the inductor spiral, R_S, was determined by EMS only for the single-layer M3-inductor. For the other structures with the very complex via arrays the number of mesh elements became too large to solve the problem in an acceptable time frame. Therefore, worst and best cases of metal thickness were calculated with EMS, and R_B was used as a fitting parameter within that data window at a given frequency. The frequency dependence of R_S due to the skin effect was considered in the model [11], [12]. The values of R_B depend on the resistivity of the silicon substrate under the inductor and on the lateral dimensions. Its order

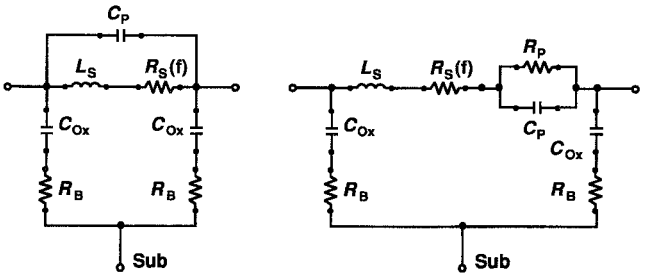

Fig. 4. Lumped element equivalent circuits for the integrated inductor (a) and MIM capacitor, (b) structures.

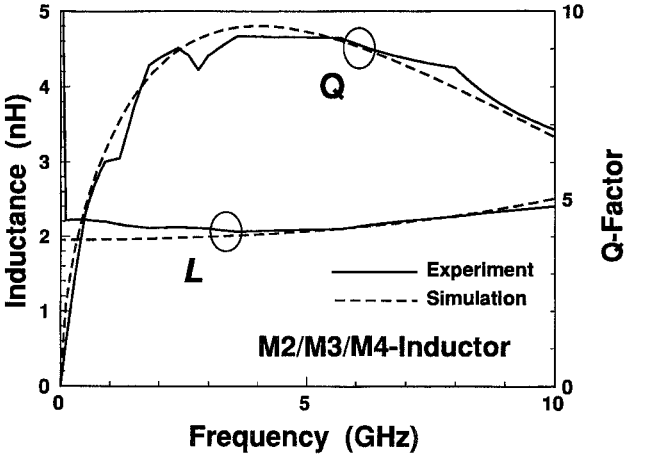

Fig. 5. Inductance and Q-factor of inductor M2/M3/M4 as a function of frequency.

of magnitude was estimated, but in the comparison with the data, R_B was used as a fitting parameter as well. The MIM capacitor model in Fig. 4 includes the device capacitance C_P, the series resistance R_S, the resistance R_P which describes the dielectric losses, the lead inductance L_S, and the substrate elements R_B and C_{OX} as described above.

The lumped element equivalent circuits in Fig. 4 were compared with the measured data by using the HP-EEsof Communication Design Suite (CDS) tool [12] for the calculation of the S_{11} parameters. Excellent agreements between measured data and models were achieved from the practical frequency range up to self-resonance as shown in Fig. 5, which is an important prerequisite for successful circuit design. The lumped element values for the different inductor and the MIM capacitor configurations, as well as the dc resistances of the inductors, are summarized in Table I. A brief summary of the measurement results can also be found in [13].

An initial evaluation of the data showed that the inductances were little dependent on the vertical configuration of the spiral structures. The inductances were also fairly independent of frequency as a result of the high self-resonance frequencies (f_{SR}). This was mainly due to the large spacing between the inductor spiral and the lossy substrate, but also a result of the sufficiently high resistivity of the bulk silicon, which gave high R_B and small C_{OX} values. Therefore, f_{SR} was mainly affected by the fringing capacitance C_P instead of the much larger C_{OX}. C_P depends on the metal spacing which was 10

TABLE I
SUMMARY OF MEASUREMENT AND EQUIVALENT CIRCUIT LUMPED ELEMENT DATA FOR THE DIFFERENT INDUCTORS AND THE MIM CAPACITOR FABRICATED

	Spiral Inductors					MIM
	M2/M3 coarse	M2/M3 dense	M2/M3/M4 dense	M3/M4 dense	M3 none	M2/M3 none
L_S /nH	2.1	2.1	1.95	2.0	2.15	0.04
R_S / Ω	4.3	4.2	3.2	3.5	5.2	0.35
C_P /pF	0.037	0.035	0.03	0.035	0.03	2.15
C_{Ox} /pF	0.18	0.18	0.18	0.12	0.18	0.39
R_B / Ω	800	800	900	850	950	20
R_{dc} / Ω	3.2	2.9	2.0	2.1	5.3	-
Q_{max}	7.4	7.6	9.3	8.6	6.5	80
$f(Q_{max})$/GHz	4	4	4	4	4.7	2.5
f_{SR} /GHz	18	18.5	20	18.5	20	>20

μm in all cases so that the values of C_P were small. Therefore, f_{SR} was much larger than the frequency of practical interest. If C_{OX} is larger and R_B is much reduced, f_{SR} can drop to the low GHz range. The inductance at the operating point then would become strongly dependent on frequency, which would make the device parameters too variable with manufacturing tolerances [7], [14]. The Q-factor was found to improve with adding additional metal layers through via arrays (M2/M3 versus M2/M3/M4 and M3 versus M3/M4 in Table I). The density of the vias did not have a significant effect on Q, at least not for the two modifications studied which are the two M2/M3-inductor modifications in Table I. The "coarse" via array covered about 30% of the length of the inductor spiral, for the "dense" via array it was about 45%. The via lengths were 15.6 μm and 20 μm, respectively.

Fig. 6 shows the maximum Q-values (Q_{max}) and the ac and dc resistances of the fabricated inductor modifications in Table I as a function of the total metal thickness. An effective metal layer thickness which could have been attributed to the via arrays was not considered because the comparison of the two M2/M3 inductors did not present any clear evidence of a significant contribution of the vias to the lateral current transport in the inductor structures. A first observation in Fig. 6 was that Q_{max} did not increase in proportion to the total metal thickness, even without consideration of the lateral current transport through the vias. The same observation was made for the ac and dc resistances which did not decrease linearly with the metal thickness. A qualitative understanding of this result is possible if one considers that in AlCu interconnect technology the tungsten (W) vias have about a three times higher resistivity than AlCu. In addition, the metal layers are typically formed in a sandwiched structure with thin metal films of higher resistivity on top and at the bottom of the AlCu film in order to overcome certain technological problems [15]. For these reasons, the M4 layer, which was

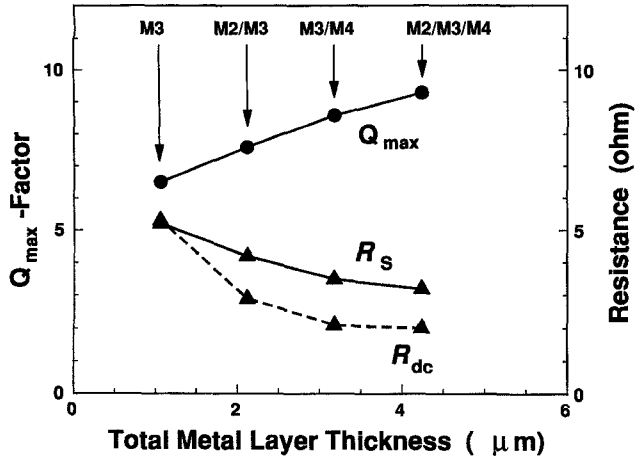

Fig. 6. The Q_{max}-factors and ac and dc resistances of the different inductor structures in Table I as function of the total metal layer thickness (not including vias).

not contacted though vias and which has the largest thickness, was conducting a major fraction of the current. This explains why the increase of Q_{max} with the total metal thickness was not as strong as one would expect.

In addition, we had fabricated the M2/M3-inductor with and without an increased substrate doping due to the p-well formation mentioned earlier in Section II to evaluate the sensitivity of Q to the substrate losses. As a result Q was reduced by nearly 15% at 2.5 GHz for the inductor with the p-well underneath, which highlights the importance of keeping the doping level under the inductor as low as possible.

With solely considering standard silicon technology, the Q_{max}-factor of close to 10 with a self-resonance at 20 GHz for the M2/M3/M4 inductor represents one of the best results published to date for monolithically integrated spiral inductors. It should be noted that this result was based on 1-port S-parameter analysis, i.e., with the substrate left floating. With a grounded substrate, Q_{max} can be somewhat lower. For an ideally grounded substrate, which is never the case due to the high substrate resistivity, Q_{max} would drop from 9.3 to 8.0 for the M2/M3/M4 inductor, based on model extrapolation. But with a resistance of the order of R_B between substrate contact and inductor, which is a more realistic assumption, Q_{max} would be reduced to about 9.0 only. In the published work on integrated inductors, similar results were achieved only by deviating from standard silicon technology. The suppression of the impact of the isolation capacitance C_{OX}, in order to keep the self-resonance frequency at high values, had been achieved before either by using micromachining techniques [14] or very high resistive substrates [16]. The inductor resistance had been lowered by using Au interconnects [16] or MCM technology for interconnections [8] which, however, does not allow an integration with submicrometer circuits on the same chip.

For the MIM capacitor a maximum Q of about 80 was measured, and the self-resonance frequency was higher than 20 GHz. The high Q_{max} was clearly a result of the two metal contacts in the MIM structures. For comparison, a MOS-capacitor which was fabricated in the same experiment had a similar capacitance value with a Q of only 3.

IV. Conclusion

The important issues to be considered for the microwave design of inductors and capacitors, which are monolithically integrated in silicon, have been highlighted in this work. Optimization based on this understanding has led to inductors with Q's approaching 10, which is one of the best results reported to date for silicon integrated inductors. The key design features were a large spacing of the inductor from the lossy silicon substrate and a reduction of the inductor resistance by shunting several layers of metal though via arrays. In spite of the good results achieved, it became clear that an inductor fabricated in a multilayer interconnect technology does not reach the Q-values possible with an equivalent one-layer structure. The inductor Q achievable in standard silicon technology seems sufficient for the fabrication of integrated broadband matching networks, but the design of narrow-band filters appears to be difficult. For monolithically integrated passive filters at 2.5 GHz and beyond, a much higher inductor Q is required. In order to be able to built such inductor structures with Qs of 30 or higher it is inevitable to deviate from standard silicon technology. Future developments of silicon MMICs should consider Au or Cu interconnects and HRS substrates or SOI wafers with very thick buried oxide layers.

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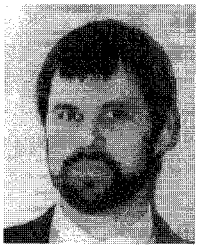

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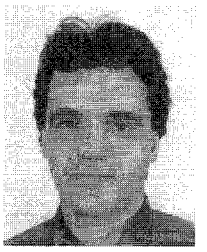

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